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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,579	03/25/2004	Michael Karl Gschwind	AUS920031084US1	7116

45327 7590 01/22/2007

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EXAMINER	
GU, SHAWN X	
ART UNIT	**PAPER NUMBER**
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,579	GSCHWIND ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,14-16,21,22,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,14-16,21,22,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This final Office action is in response to the amendment filed 21 November 2006. Claims 1-8, 14-16, 21, 22, 26 and 27 are pending. Claims 9-13, 17-20 and 23-25 have been cancelled. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 26 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Patterson and Hennessy [Computer Architecture: A Quantitative Approach] (hereinafter "Patterson").

Per claim 26, Patterson teaches a method for providing needed data to a processing element, the method comprising:

receiving the needed data and coherence directory data corresponding to the needed data;

using the received coherence directory information to determine a condition of the need data;

determining if the condition of the needed data is compatible with a required access mode ("exclusive state", see page 682, fourth paragraph);

in the event the condition of the needed data is compatible with required access mode, providing the needed data to the processing element (see pages 682-685, see Fig 8.24 and 8.25 and the corresponding paragraphs explaining the figures; see page 682, fourth paragraph, "any cache block must be in the exclusive sate when it is written and any shared block must be up to date in memory; the processing element is interpreted as the combination of Patterson's processor, cache and directory controller).

Per claim 27, Patterson further teaches in the event the condition of the needed data is not compatible with the required access mode, performing at least one coherence action (see fig 8.25 and pages 682-685, during write, if the block is not in exclusive mode, a coherence/state change action is performed).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8, 14-16, 21, 22, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson and Hennessy [Computer Architecture: A

Quantitative Approach] (hereinafter "Patterson") and Williams et al. [US 6,993,630 B1] (hereinafter "Williams").

Per claim 1, Patterson teaches a processing system, comprising:

a memory comprising a coherence directory and associated coherence directory data, wherein the coherence directory comprises a plurality of memory blocks each having difference corresponding coherence directory data (Fig.8.22 and page 680, first paragraph, "a bit vector for each memory block");

a plurality of buffers interconnected to said memory (Fig 8.22, caches);

a plurality of processing elements (Fig 8.22, combination of processor and directory controller, see page 682, fourth paragraph), each said processing element interconnected to a different one of said plurality of buffers (see Fig 8.22);

wherein each of the processing elements comprises requesting means for requesting a selected one of said memory blocks from said memory (see Fig 8.24 and 8.25, and pages 682-685);

wherein the memory comprises means responsive to said requesting means for providing the selected memory block and the coherence directory data corresponding to the selected memory block to a requesting one of said processing elements (messages sent among nodes to maintain coherence, see page 681 and Fig.8.23, the memory data request must also be serviced as well, see page 682, last paragraph; and page 682, fourth paragraph, a processor requests memory for a write operation, the block is cached, its coherence directory value is tested to verify its 'exclusiveness', also see Fig

8.24 and 8.25, pages 683-685, 'write miss', volumes are sent to the owner processor, while the corresponding directory values are sent/written/updated to the directory. The claims only stated that 'memory block' and 'coherence directory data' are sent to the processing element, but the claims did not state in what order they are sent); and

wherein each of the processing elements comprises means for receiving the selected memory block and the coherence directory corresponding to the selected memory block (see citation and notes set forth above), and is configured to determine if the selected memory block is available for a particular access mode (page 682, fourth paragraph, "any cache block must be in the exclusive state when it is written and any shared block must be up to date in memory"; also the rejections of claims 26 and 27 set forth above).

Patterson does not specifically disclose a plurality of prefetch address registers, providing the contents of at least one of the prefetch address registers to a requesting processing element, and each of the processing element comprising means for receiving the contents of the at least one of the prefetch registers.

However, Williams teaches a method implementing a directory based coherence protocol supporting the presence of prefetch address registers (Secondary Level Cache 108, see Williams, Figs 1-3, and General Register Array 300, see Williams, Fig.3, Col.9, lines 60-67 and Col.10, lines 4-40), providing the contents of at least one of the prefetch address registers to a requesting processing element and each of the processing element comprising means for receiving the contents of the at least one of the prefetch registers (GRA 300 contains the prefetch request address, see Williams, Col.9, lines 56-

67 and Col.10, lines 4-59; the Pre-fetch control logic 304 is considered to be part of the processing element after combining the teachings of Patterson and Williams, and 304 performs pre-fetching by processing the requests stored with GRA 300 and provided to the Pre-fetch logic 304). The motivation presented by Williams for incorporating the above limitations is reducing the latency associated with data retrieval (see Williams, Col.6, lines 63-66). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to include Williams' limitations with Patterson's teachings for the same motivation described by Williams.

Per claims 2 and 21, Patterson further teaches that the processing elements are connected with said buffers via point to point links (see Fig 8.22) and the requesting of the memory blocks and the generating and receiving of the responses are carried out by sending and receiving data over point to point links (the messages and replied data values are sent between the processors and the directories, with a single source and a single destination, hence point-to point links; see page 681, lines 5-16).

Per claim 3, Patterson in view of Williams further teaches the contents of the at least one prefetch address register is a field in a response (since the contents of the register is provided to a processing element as described in claim 1, they must be a field in a response).

Per claim 4, Patterson in view of Williams further teaches the contents of the at least one prefetch address register is included in a transmitted directory information modifier (since the contents of the register is provided to a processing element as described in claim 1, they must be a field in a response; the transmitted directory information modifier is broadly interpreted as a response, since it is defined by the Applicant's disclosure).

Per claim 5, Patterson in view of Williams further teaches the memory comprises means responsive to said requesting means for providing a plurality of memory blocks including the selected memory block, the coherence directory data corresponding to the plurality of memory blocks (see Patterson, pages 682-685), and contents of at least one of the prefetch address registers to a requesting one of said processing elements (see claim 1's rejection by Patterson in view of Williams set forth above, also see claim 16's rejection).

Per claim 6, Patterson in view of Williams further teaches the plurality of memory blocks and the coherence directory data corresponding to the plurality of memory blocks are stored in a prefetch buffer (Patterson in view of Williams teaches prefetching memory), and the contents of the at least one of the prefetch address register comprises an identifying address of said plurality of memory blocks (see Williams, col.10, ln.4-40, GRA stores the request addresses).

Per claim 7, Patterson in view of Williams further teaches each of the processing elements is configured to use a prefetched plurality of memory blocks stored in a prefetch buffer to provide memory data if said coherence directory data corresponding to the selected memory block indicates the selected memory block is available for either: (i) a shared access mode, or (ii) both the shared access mode and an exclusive access mode (see Patterson, "An Example Directory Protocol", pages 682-685, and page 682, fourth paragraph, "any cache block must be in the exclusive state when it is written and any shared block must be up to date in memory").

Per claim 8, Patterson in view of Williams further teaches the identifying address stored in said at least one prefetch register indicates that said plurality of memory blocks is available for either: (i) the shared access mode, or (ii) for both the shared access mode and the exclusive access mode (see arguments presented in claim 7's rejection set forth above; also the address in GRA taught by Williams indicates the requested memory blocks).

Per claims 14, Patterson teaches a method for providing memory data to a requestor of the memory data, the method comprising:

requesting a memory block from a memory hierarchy level having a coherence directory and associated coherence directory data (cache, memory and directory, see page 680, Fig.8.22);

generating a response including the memory data and corresponding coherence directory data (messages sent among nodes to maintain coherence, see page 681 and Fig.8.23, the memory data request must also be serviced as well, see page 682, last paragraph; and Fig 8.24-8.25, pages 683-685; also see claim 1's rejection as set forth above);

updating directory coherence data corresponding to the memory data (see Fig 8.25 and pages 682-685, during write, if the block is not in exclusive mode, a coherence/state change action is performed, also see rejection of claim 27 as set forth above),

receiving the response including the memory data and the corresponding coherence directory data from said memory hierarchy level (messages sent among nodes to maintain coherence, see page 681 and Fig.8.23, the memory data request must also be serviced as well, see page 682, last paragraph),

determining whether the received coherence directory data is compatible with a required access mode (see the rejection of claim 26 as set forth above);

performing at least one coherence action if the received coherence directory data is incompatible with the required access mode (see claim 27's rejection as set forth above),

providing the memory data to the requestor of memory data (see pages 682-685, also see "write miss" on page 685).

Patterson does not specifically disclose having prefetch address registers, and indicating the address of a prefetched block in a prefetch address register.

However, Williams teaches a method implementing a directory based coherence protocol supporting the presence of prefetch buffers (Secondary Level Cache 108, see Williams, Figs 1-3), a memory hierarchy level having prefetch address registers (General Register Array 300, see Williams, Fig.3, Col.9, lines 60-67 and Col.10, lines 4-40), and indicating the address of a prefetched block in a prefetch address register (GRA 300 contains the prefetch request address, see Williams, Col.9, lines 56-67 and Col.10, lines 4-59; the Pre-fetch control logic 304 is considered to be part of the processing element after combining the teachings of Patterson and Williams, and 304 performs pre-fetching by processing the requests stored with GRA 300 and provided to the Pre-fetch logic 304). The motivation presented by Williams for incorporating the above limitations is reducing the latency associated with data retrieval (see Williams, Col.6, lines 63-66). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to include Williams' limitations with Patterson's teachings for the same motivation described by Williams.

Per claim 15, Patterson in view of Williams further teaches the providing comprises providing the memory data and the coherence directory data to a requestor of the memory data (see the arguments and citations set forth in claims 1 and 14; the requestor includes the directory, the directory controller and the requesting processing, also see Patterson, page 685, "write miss").

Per claim 16, Patterson in view of Williams does not specifically teach that the provided coherence directory data comprises merged coherence data generated by combining information contained in at least one coherence directory entry and at least one prefetch address register. However, it is clear that combining multiple pieces of response information into one information reduces communication overhead and the number of communication transactions over the network and thereby reduces the network load. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to merge coherence data generated by combining information contained in at least one coherence directory entry and at least one prefetch address register in order to reduce overhead, the number of transactions, and the network load.

Per claim 22, Patterson in view of Williams further teaches at least one of the prefetch address registers stores a prefetch address and a prefetch data length (address and data signals are stored in GRA, see Williams, Col.9, lines 59-65).

Response to Arguments

6. Applicant's arguments filed on 21 November 2006 regarding claims 1-8, 14-16, 21, 22, 26 and 27 have been considered but they are not persuasive. The claims are taught by Patterson in further view of Williams as set forth above.

With regard to the Applicant's argument on pages 13-14 of the Applicant's response discussing the rejection of claim 14. The Applicant's argument states that

"None of the messages sent among nodes to maintain coherence described by Patterson on page 681 and Fig 8.23 include 'memory data and corresponding coherence directory data'". However, on page 682, and specifically in the fourth and fifth paragraphs and page 685, the paragraphs beginning with "write miss", Patterson clearly teaches sending both the memory data and the corresponding coherence directory data to the processing element. The processing element is designated as the combination of the processor and the directory controller as set forth above in the rejections of claims 1, 14 and 26. The directory controller and the directory receives the coherence data as well as the requested block, and forward the block to the requesting processor.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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12 January 2007